IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application: Y. KAWAMURA et al

Serial No. 09/754,193 Filed: January 5, 2001

Group Art:

3723

Examiner:

M. Rachuba

For:

METHOD FOR POLISHING SURFACE OF SEMICONDUCTOR DEVICE SUBSTRATE

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents Mail Stop Patent Application P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, the Applicants inform the Examiner of the documents cited during prosecution of the parent application, USSN 09/754,193.

The Applicants request the Examiner to initial and return a copy of the attached PTO-1449 form as an indication that the references have been considered.

Respectfully submitted,

Shainath Malur

Registration No. 34,663

Attorney of Record

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Date: September 12, 2003

FORM PTO-1449 (REV. 7-80)			U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		E ATTY. DOCKET NO. E ASA - 955 - 02	SERIA	SERIAL NO.			
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